HC5518XEVAL Evaluation Board User's Guide

Application Note | September 2000 | AN9814.2

Introduction

The HC5518XEVAL evaluation board provides a complete evaluation system for the HC55185 family of ringing SLICs. The evaluation board design consists of the HC55185 device application circuit, a single +5V CODEC for line circuit evaluations and on board logic for stand alone operation. The evaluation boards have been designed to support back to back operation, providing further insight to the complete signal path and solution.

The transient behavior of the SLIC in response to mode changes has been significantly improved with the HC55185 design. The benefit to the application is reduction or more likely elimination of $\overline{DET}$ glitches when off hook events occur. In addition to internal circuit modifications, the change of the C_{FB} value contributes to this functional improvement. Please reference the HC55185 data sheet for detailed information regarding this feature.

Voltage ratings for external components have been selected based on 100V device operation, therefore compatibility to lower voltage versions is guaranteed.

Getting Started

Your evaluation kit should contain this user's guide and the following hardware.

1. One HC5518XEVAL evaluation board.
2. At least one HC55185 device sample, already in board.
3. One PLCC extraction tool.
4. One cable assembly with multi colored conductors.
5. One cable assembly with solid white conductors.

The evaluation board should have the same appearance as the silk screen shown in Figure 1.

Applying Power to the Evaluation Board

Here are a few safeguards with power sequencing until you are accustomed to using the high voltages required by the devices.

1. Limit the current on all power supplies to 100mA.
2. Turn on the power supplies after the power cables are attached to the evaluation boards.

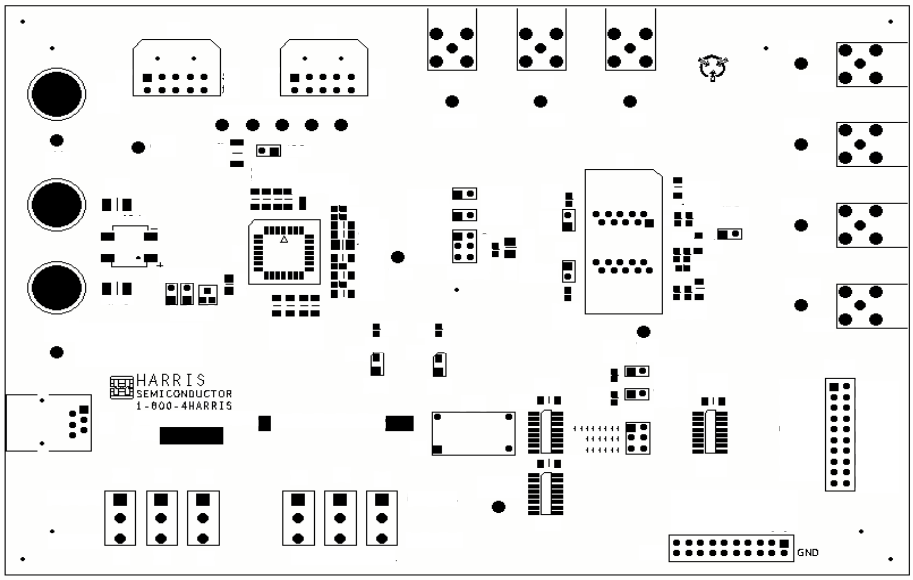


FIGURE 1. EVALUATION BOARD SILK SCREEN

Evaluation Board Functional Description

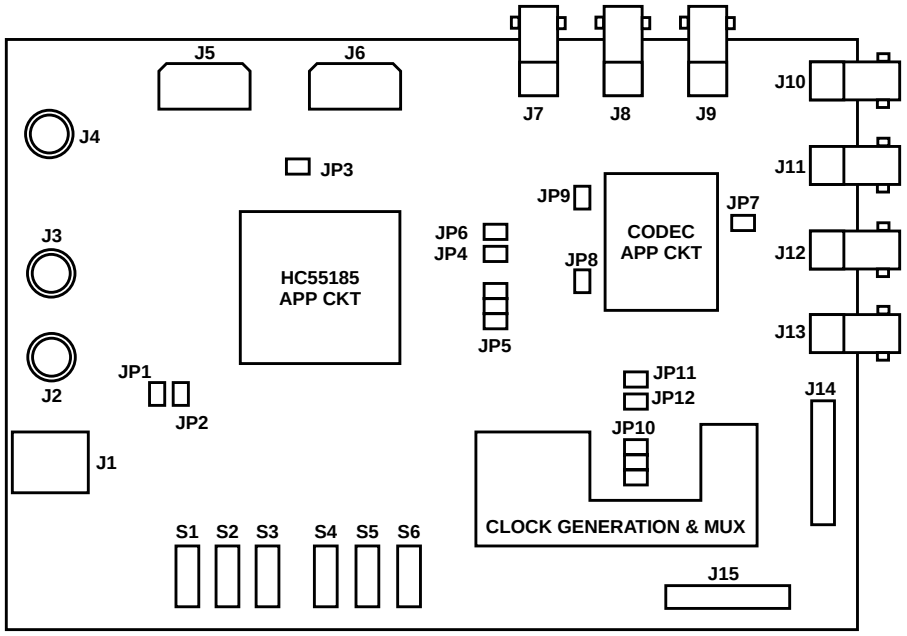


FIGURE 2. EVALUATION BOARD FUNCTIONAL DIAGRAM

Evaluation Board Jumper Definitions

JUMPER	DESCRIPTION
JP1	Connects SW- directly to the device Ring terminal of device. Used in conjunction with external load D_{TA} and R_{TA}.
JP2	Connects SW+ through test load to the Tip terminal of device. Used in conjunction with external load D_{TA} and R_{TA}.
JP3	Connects the VBH to VBL terminal. Should be used with devices without battery switch.
JP4	Connects the receive output of the CODEC (U6) to the device receive input VRX. Path is AC coupled with C_{RX}.
JP5	Position1, CODEC: Connects the CODEC receive output to the device ringing input. Path is AC coupled by C_{RS}.
	Position 2, EXT: Connects the VRS connector J9 to the device ringing input. Path is AC coupled by C_{RS}.
	Position 3 TRAP: Connects the VRS connector J9 thru RC network to the device ringing input. Path is AC coupled.
JP6	Connects the device transmit output VTX to the CODEC amplifier for transhybrid balance. Path is AC coupled by C_{TX}.
JP7	Connects the receive output of CODEC to transhybrid amplifier, AC coupled by C_1. Normally inserted for proper operation.
JP8	Inserting jumper sets the CODEC to A-law coding. Open sets the CODEC to μ-law coding.
JP9	Inserting jumper powers down the CODEC. Open provides normal CODEC operation.
JP10	Position 1: Sets the CODEC master clock to 2.048MHz.
	Position 2: Sets the CODEC master clock to 512kHz
	Position 3: Sets the CODEC master clock to 256kHz.
JP11	Enables the on board logic multiplexer. Should be installed for single board or back to back evaluations. Remove when driving BNCs J10 thru J13.
JP12	Inserting jumper selects on board clock and frame sync generator. Insert to configure board as master for back to back evaluations or for single board evaluations. Remove to configure board as slave for back to back evaluations.

Test Points

Each connector interface to the evaluation board has a test point. All test points are DC coupled and should be guarded against ground shorts. High impedance test inputs, such as oscilloscopes or DVMs, should be used to monitor these points. Unused BNC connections also provide convenient test point access.

Toggle Switches

The six toggle switches, S1 thru S6, interface directly to the HC55185 device. Positioning any switch towards the top of the board is a logic “1”. Positioning any switch towards the bottom of the board is a logic “0”. All switches are labeled with the control signal name of the HC5518x device.

The switch E0 selects the switch hook (E0 = 1) or the ground key detector (E0 = 0) to appear at $\overline{DET}$. During ringing, the device overrides E0 and sends the ring trip detector to $\overline{DET}$. The switched labeled $\overline{SWC}$ turns on the uncommitted switch when set to a logic low. The battery select signal BSEL, selects the high battery when set to logic high. The operating modes for the HC55185 device are provided in Table 1.

TABLE 1. HC55185 OPERATING MODES

OPERATING MODE	F2	F1	F0
Low Power Standby	0	0	0
Forward Active	0	0	1
Unused	0	1	0
Reverse Active	0	1	1
Ringing	1	0	0
Forward Loop Back (Note)	1	0	1
Tip Open	1	1	0
Power Denial	1	1	1

NOTE: The HC55185 device should always operate from low battery voltage when using the Forward Loop Back mode.

Refer to the device electrical data sheet for detailed descriptions regarding each operating mode according to the device under evaluation.

Evaluation Board Connector Descriptions

CONNECTOR	DESCRIPTION
J1	RJ11 type phone connector.
J2	Ring terminal of board.
J3	Tip terminal of board.
J4	Grounding lug connected to board ground plane.
J5	1: V_{CC}. Positive 5V supply to CODEC U6, clock generator U5 and logic devices U2 thru U4 (red wire).
	2: V_{BH}. High negative battery supply to the HC55185 device (orange wire).
	3: V_{BL}. Low negative battery supply to the HC55185 device (yellow wire).
	4: +5V. Positive 5V supply to the HC55185 device and LEDs (green wire).
	7 thru 10: GND. Twisted pair returns for external supply connections (black wires).
J6	Identical pinout as J5. Either connector provides daisy chain connection to second board for back to back evaluation.
J7	Transmit analog output from HC55185 device, VTX. This path is AC coupled by C_{TX}.
J8	Receive analog input to HC55185 device, VREC. This path is AC coupled by C_{RX}.
J9	Ringing input to HC55185 device, VRS. This path is AC coupled by C_{RS}.
J10	Serial transmit data output of CODEC U6.
J11	Serial receive data input to CODEC U6.
J12	Common frame sync input for receive and transmit digital data.
J13	Common clock for CODEC data transfer and conversion.
J14	20 pin, 100 mil spacing header with all digital PCM data interfaces to CODEC U6.
J15	20 pin, 100 mil spacing header with all digital interfaces to HC55185 device.

Stand Alone Configuration

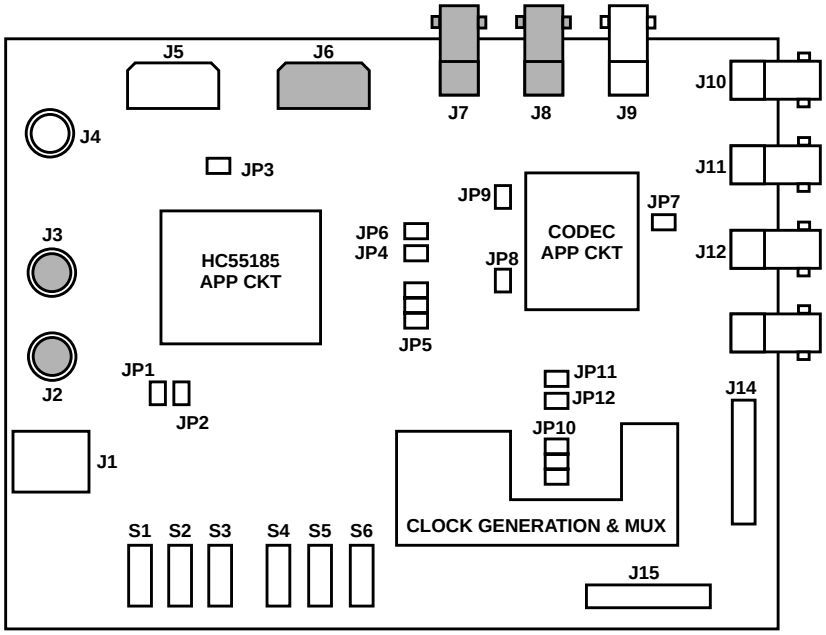


FIGURE 3. STAND ALONE CONNECTORS AND JUMPERS

Description

The stand alone configuration supports any measurement of the HC55185 device. With all the jumper locations open, the device is totally isolated from all other active circuitry on the evaluation board. All other circuitry is powered, but does not interfere with proper SLIC operation.

Power Supply Connections

Power should be applied to the evaluation board using the primary power cable. Either J5 or J6 may be used. Prior to applying power, the voltage setting of each supply should be verified. The power supplies should be turned off while mating the primary power cable to the evaluation board.

Jumper Settings

All jumper positions should be open for the stand alone configuration.

Measurement Capability

Nearly all AC and DC parameters of the device can be measured using this configuration. The device has been socketed to allow easy measurements of more than a single device. An extraction tool has been included with the evaluation kit and should be used to remove the device from the socket. The typical device measurements are listed below.

3. Power supply current per operating mode.
4. Tip and Ring DC voltages per operating mode.
5. On hook AC gains G_{42}, G_{24} and G_{44}.
6. Off hook AC gains G_{42}, G_{24} and G_{44}.
7. Other AC parameters such as longitudinal balance.

Status LEDs

The status LEDs $\overline{DET}$ and $\overline{ALM}$ are active for the stand alone configuration. $\overline{DET}$ should only light when a DC current path exists from Tip to Ring or during forward loop back. $\overline{ALM}$ should only light during forward loop back operation. Normal device evaluations should not cause the $\overline{ALM}$ indicator to light.

Uncommitted Switch Jumpers

When the jumpers JP1 and JP2 are installed, the uncommitted switch is connected across Tip and Ring. The test load of D_{TA} and R_{TA} will connect across the Tip and Ring terminals when the uncommitted switch is turned on. The DC load will result in $\overline{DET}$ transitioning to a logic low. The circuit diagram is shown below.

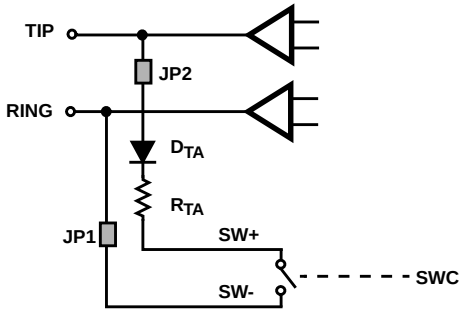


FIGURE 4. TEST LOAD SWITCHING

Socket Removal

The surface mount socket for the HC55185 device has the same solder foot print as the PLCC package. Therefore, the socket may be removed for more extensive characterization.

Stand Alone Configuration Typical Measurements

Supply Currents (milli amps) - On Hook

OPERATING MODE	F2, F1, F0	E0	SWC	BSEL	ICC	IBH	IBL	I+5V
Low Power Standby	0, 0, 0	x	1	1	29	0.4	0.1	3.5
Forward Active	0, 0, 1	x	1	0	29	0	1.0	4.0
Unused	0, 1, 0	n/a	n/a	n/a	n/a	n/a	n/a	n/a
Reverse Active	0, 1, 1	x	1	0	29	0	1.3	4.2
Ringing	1, 0, 0	x	1	1	29	1.8	0.4	7.2
Forward Loop Back	1, 0, 1	x	1	0	29	0	19	20
Tip Open	1, 1, 0	x	1	1	29	0.4	0.1	4.0
Power Denial	1, 1, 1	x	1	x	29	0	0.3	3.4

NOTE: The current I+5V includes the current flowing through the $\overline{DET}$ and $\overline{ALM}$ LEDs when they are on.

Tip and Ring Voltages (Volts) - On Hook

OPERATING MODE	F2, F1, F0	E0	SWC	BSEL	TIP	RING
Low Power Standby	0, 0, 0	x	1	1	-0.6	-49
Forward Active	0, 0, 1	x	1	0	-4.0	-19.4
Unused	0, 1, 0	n/a	n/a	n/a	n/a	n/a
Reverse Active	0, 1, 1	x	1	0	-19.4	-4.0
Ringing	1, 0, 0	x	1	1	-50	-50
Forward Loop Back	1, 0, 1	x	1	0	-4.4	-19
Tip Open	1, 1, 0	x	1	1	Float	-49
Power Denial	1, 1, 1	x	1	x	Float	Float

AC Gains (dB), Off Hook, 600Ω Termination - Forward and Reverse Active Only

OPERATING MODE	F2, F1, F0	E0	SWC	BSEL	G_{42}	G_{24}	G_{44}
Forward Active	0, 0, 1	x	1	0	0.0	-7.3	-7.3
Reverse Active	0, 1, 1	x	1	0	0.0	-7.3	-7.3
AC Gain Equations	G_{42} $G_{42} = -2\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right)$		G_{24} $G_{24} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right)$		G_{44} $G_{44} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right)$		

Ringing Configuration

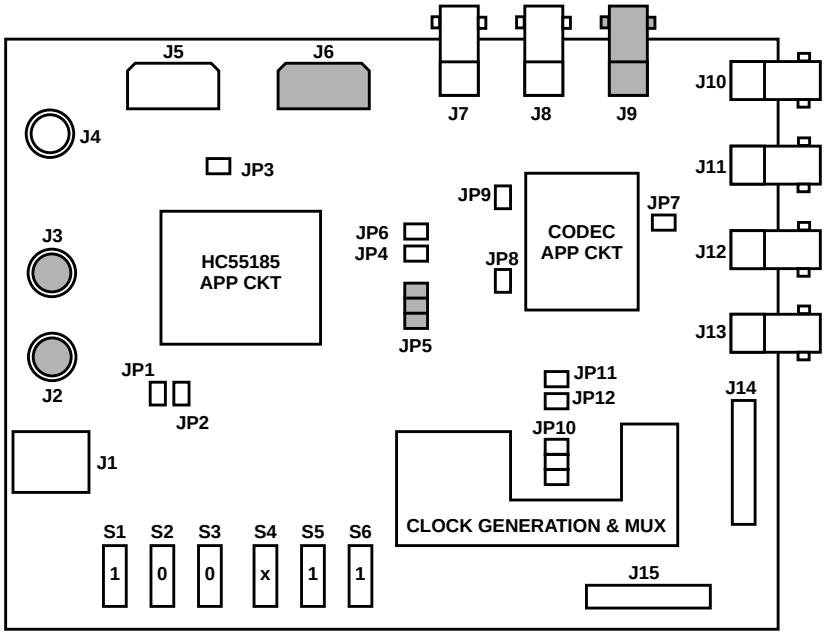


FIGURE 5. RINGING CONNECTORS AND JUMPERS

Description

The ringing configuration supports full evaluation of the ringing capability of the HC55185 device. The evaluation board design does not include a 20Hz digital code generator, therefore, all ringing waveforms will be sourced by external test equipment.

Power Supply Connections

Power should be applied to the evaluation board using the primary power cable. Either J5 or J6 may be used. Prior to applying power, the voltage setting of each supply should be verified. The power supplies should be turned off while mating the primary power cable to the evaluation board.

Jumper Settings

The jumper JP5 provides three positions for different ringing techniques.

TABLE 2. JP5 JUMPER POSITIONS

JP5 POSN	DESCRIPTION
CODEC	Connects the CODEC receive output to the device ringing input. Signal path is AC coupled.
EXT	Connects the VRS connector J9 to the device ringing input. Signal path is AC coupled.
TRAP	Connects the VRS connector J9 thru RC network to the device ringing input. Signal path is AC coupled.

CODEC Ringing

Most test equipment designed to evaluate the CODEC PCM interface are capable of output frequencies as low as 20Hz. If such a piece of equipment is available, then CODEC ringing can be evaluated. The digital interface to the CODEC would be provided by the BNC connectors J10 thru J13. Verify JP11 is open prior to driving signals into the BNC connectors. An output level of 0dBm from the CODEC will provide full scale ringing when operating from -100V battery.

External Ringing Source

Using an external function generator at J9 provides the most control of the ringing waveform. The flexibility of the ringing interface can be fully exercised by the function generator. To evaluate DC offsets during ringing, the capacitor C_{RS} must be shorted. Most functions generators provide DC offset as part of the output waveform. Positive DC offsets on VRS move Tip towards ground and Ring towards battery.

Trapezoidal Ringing

A logic level square wave, at J9, with 50% duty cycle will be shaped by the components R_{TRAP} and C_{TRAP} when this jumper position is selected. The components shipped with the evaluation board will result in a $75V_{RMS}$ trapezoidal ringing waveform when operating from a -100V battery.

Ring Trip Control

Three very distinct actions occur when the devices detects a ring trip. First, the $\overline{DET}$ output is latched low. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the VRS input is disabled, removing the ring signal from the line. Third, the device is internally forced to the forward active mode. The low battery is not automatically selected upon ring trip.

Digital Loop Back Configuration

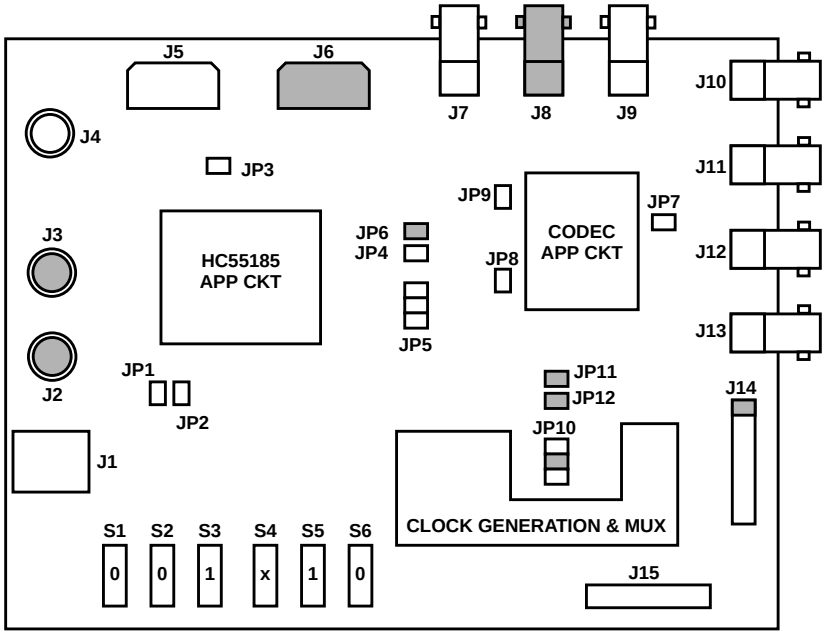


FIGURE 6. DIGITAL LOOP BACK CONNECTORS AND JUMPERS

Description

The digital loop back configuration verifies the interface and operation of the HC55185 device and the CODEC. This configuration provides a self test to verify proper operation of the board. In addition, it provides a complete digital loop, allowing analog control of the digital input and output of the CODEC. Forward active and reverse active or teletax will support the digital loop back configuration.

Power Supply Connections

Power should be applied to the evaluation board using the primary power cable. Either J5 or J6 may be used. Prior to applying power, the voltage setting of each supply should be verified. The power supplies should be turned off while mating the primary power cable to the evaluation board.

Jumper Settings

All jumper settings and functions are described below.

TABLE 3. DIGITAL LOOP BACK JUMPER POSITIONS

JUMPER	DESCRIPTION
JP6	Connects the device transmit output VTX to the CODEC amplifier for transhybrid balance.
JP10, POSN 2	Sets the CODEC master clock to 512kHz.
JP11	Enables the on board logic multiplexer.
JP12	Inserting jumper selects on board clock and frame sync generator.
J14, POSN 1	Connects the CODEC digital output DT to digital input DR.

Signal Flow

Driving a signal at VREC, J8, will result in a signal from the CODEC receive output when the HC55185 device is terminated at Tip and Ring. The following diagram shows the signal path formed by the jumpers and terminated SLIC.

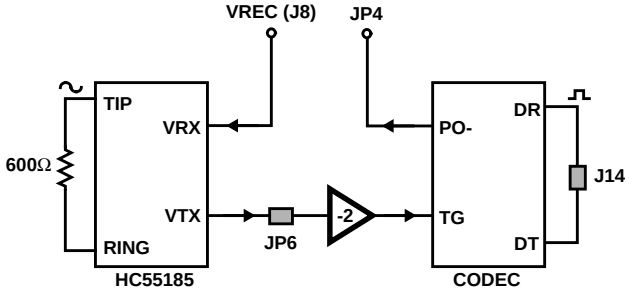


FIGURE 7. DIGITAL LOOP BACK SIGNAL FLOW

With VREC input signal level of $0.775V_{RMS}$, a signal level of $0.337V_{RMS}$ should result at the VTX output when terminated with 600Ω. The signal level at VTX is determined by the 4-wire to 4-wire gain, G_{44}, of the HC55185. The transhybrid balance is not connected, therefore, the digitized signal level at the CODEC will be approximately $0.674V_{RMS}$. The CODEC transfer functions are set for unity gain, therefore the signal level at PO- should be approximately $0.674V_{RMS}$.

The signal levels for digital loop back are independent of the clock selected by JP10.

Refer to the device electrical data sheet for the design equations for the 4-wire to 4-wire gain as a function of termination and synthesized impedance.

PCM4 Configuration

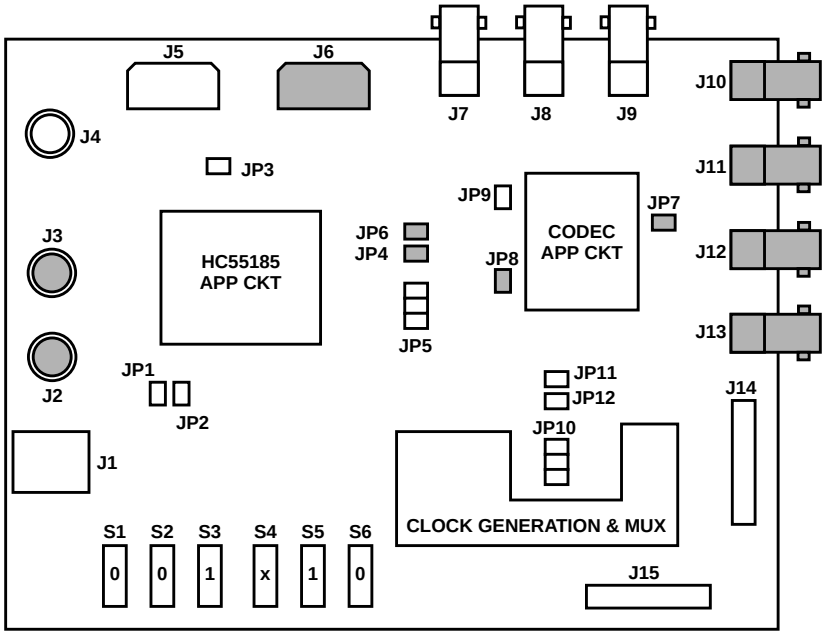


FIGURE 8. PCM4 CONNECTORS AND JUMPERS

Description

The PCM4 configuration verifies the AC transmission of the HC55185 and CODEC. Any piece of test equipment capable of PCM testing with digital and analog interfaces can be used in this configuration.

Power Supply Connections

Power should be applied to the evaluation board using the primary power cable. Either J5 or J6 may be used. Prior to applying power, the voltage setting of each supply should be verified. The power supplies should be turned off while mating the primary power cable to the evaluation board.

Jumper Settings

All jumper settings are described below.

TABLE 4. PCM4 JUMPER POSITIONS

JUMPER	DESCRIPTION
JP4	Connects the receive output of the CODEC (U6) to the device receive input VRX. Signal path is AC coupled.
JP6	Connects the device transmit output VTX to the CODEC amplifier for transhybrid balance. Signal path is AC coupled.
JP7	Connects the receive output of CODEC to transhybrid amplifier, AC coupled by C1.
JP8	Inserting jumper set the CODEC to A-law coding. Open sets the CODEC to μ-law coding. **This must match PCM test equipment coding scheme for proper operation.**

Clock and Frame Sync

The clock and frame sync signals are driven at connectors J13 and J12 respectively. The clock input is common to the MCLK, BCLKT and BCLKR of the CODEC. The frame sync input is common to the receive and transmit frame syncs, FSR and FST, of the CODEC. These connections define synchronous mode of operation.

Digital to Analog

The receive signal path is defined from the CODEC PCM input to the HC55185 Tip and Ring outputs. The PCM4 tester is capable of driving digital test signals on the PCM bus and measuring the resultant signal at Tip and Ring. With this type of capability, the full receive path can be evaluated. Typical performance measurements include overall loss, gain variation versus frequency, gain versus signal level and 2-wire return loss. In addition fidelity measurements such as idle channel noise and distortion are also performed.

Analog to Digital

The transmit signal path is defined from HC55185 Tip and Ring interface to the CODEC PCM output. The same tests performed for the receive path also apply to the transmit path.

Digital to Digital

The digital to digital path is from the CODEC PCM input to the CODEC PCM output. This signal path provides a measure of the transhybrid balance for the line circuit. Most other AC performance metrics are base on analog to digital or digital to analog measurements. For proper transhybrid measurements, verify jumper JP7 is inserted.

PCM4 Configuration Typical Measurements

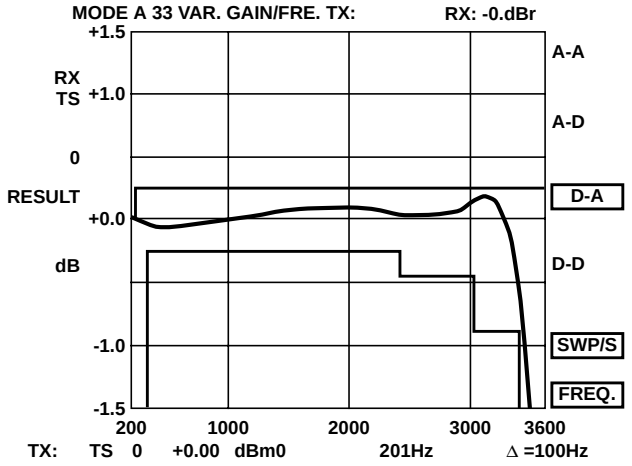


FIGURE 9. DIGITAL TO ANALOG GAIN vs FREQUENCY

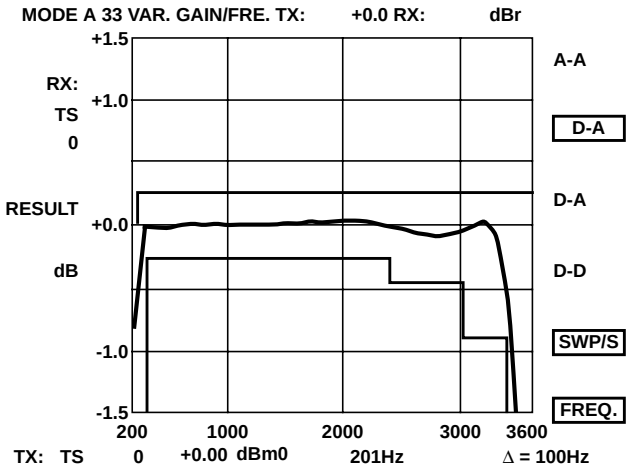


FIGURE 10. ANALOG TO DIGITAL GAIN vs FREQUENCY

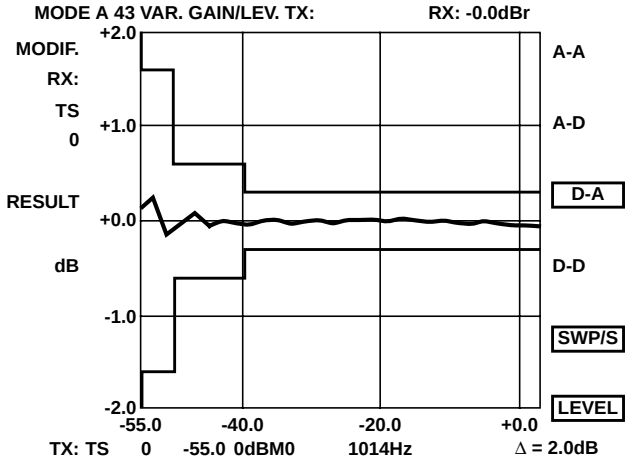


FIGURE 11. DIGITAL TO ANALOG GAIN vs LEVEL

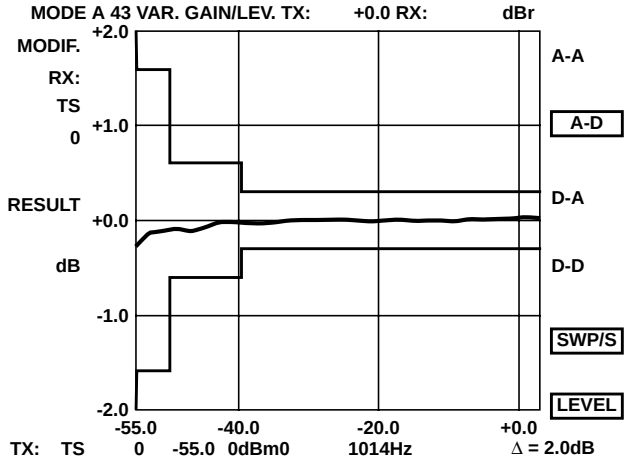


FIGURE 12. ANALOG TO DIGITAL GAIN vs LEVEL

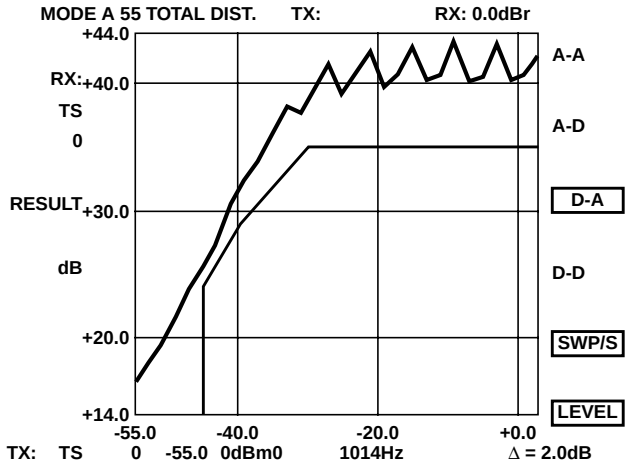


FIGURE 13. DIGITAL TO ANALOG TOTAL DISTORTION

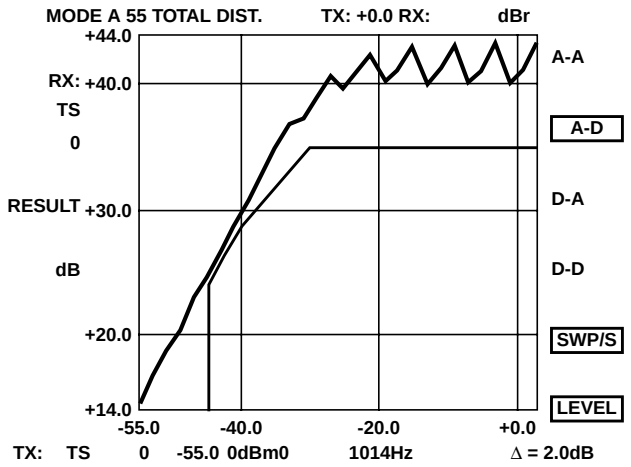


FIGURE 14. ANALOG TO DIGITAL TOTAL DISTORTION

Back to Back Configuration

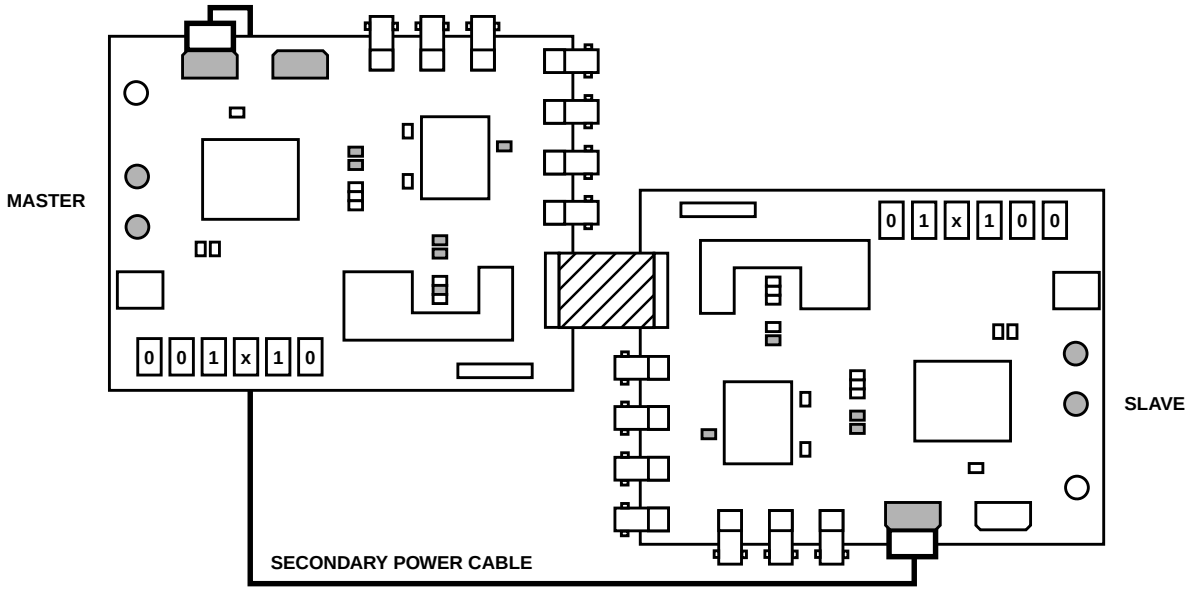


FIGURE 15. BACK TO BACK CONNECTORS AND JUMPERS

Description

The back to back configuration connects two evaluation boards together at the PCM interface. The PCM output data from one board is the PCM input data to the other board. One board is configured as a master for clock generation and the other is configured as a slave. A secondary power cable provides daisy chain power to the second evaluation board.

Power Supply Connections

Power should be applied to the evaluation board using the primary power cable. Either J5 or J6 may be used. Prior to applying power, the voltage setting of each supply should be verified. The power supplies should be turned off while mating the power cables to the evaluation boards.

Jumper Settings

. All jumper settings are described below.

TABLE 5. MASTER BOARD JUMPER POSITIONS

JUMPER	DESCRIPTION
JP4	Connects the receive output of the CODEC (U6) to the device receive input VRX.
JP6	Connects the device transmit output VTX to the CODEC amplifier for transhybrid balance.
JP7	Connects the receive output of CODEC to transhybrid amplifier, AC coupled by C1.
JP10, POSN 2	Sets the CODEC master clock to 512kHz.
JP11	Enables the on board logic multiplexer.
JP12	Configures board as master.

TABLE 6. SLAVE BOARD JUMPER POSITIONS

JUMPER	DESCRIPTION
JP4	Connects the receive output of the CODEC (U6) to the device receive input VRX.
JP6	Connects the device transmit output VTX to the CODEC amplifier for transhybrid balance.
JP7	Connects the receive output of CODEC to transhybrid amplifier, AC coupled by C1.
JP11	Enables the on board logic multiplexer.

In this configuration the master board provides the clock and frame sync to the slave board. The selection of the clock rate is arbitrary and may be any of the available frequencies.

The ribbon cable used to connect the two boards at J14 also connects the ground planes of the two evaluation boards. Having returns adjacent to the high speed clock edges is critical to reducing board level noise.

If transmission quality is poor verify both master and slave boards are set up for same coding scheme, JP8. In addition, verify the transhybrid jumper, JP7, is inserted in both boards. If signal quality still does not improve, verify JP12 of the slave board is not populated.

Analog to Analog Verification

The back to back configuration verifies the complete signal path of two evaluation boards. Full duplex transmission is provided from one Tip and Ring interface to the other. Both HC55185 devices do not have to be in the same transmission mode (forward, reverse or teletax) for proper back to back operation.

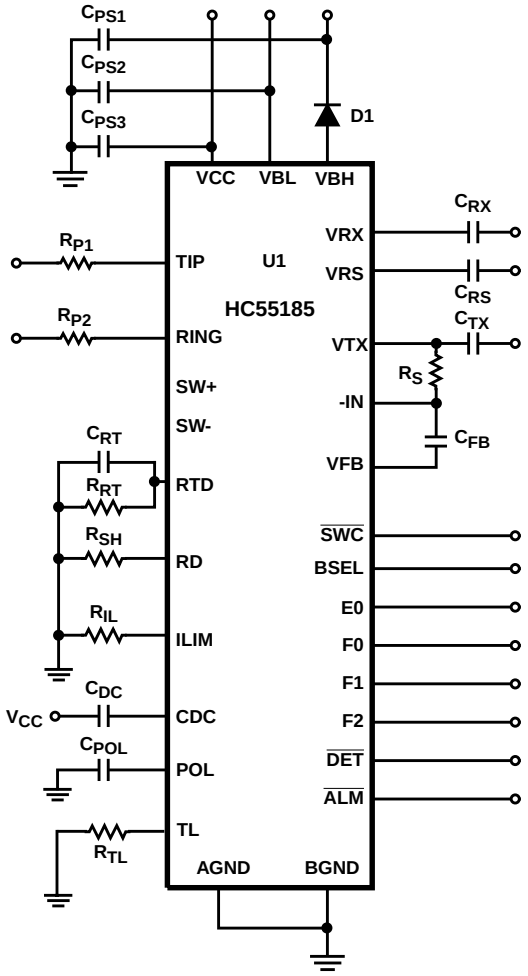


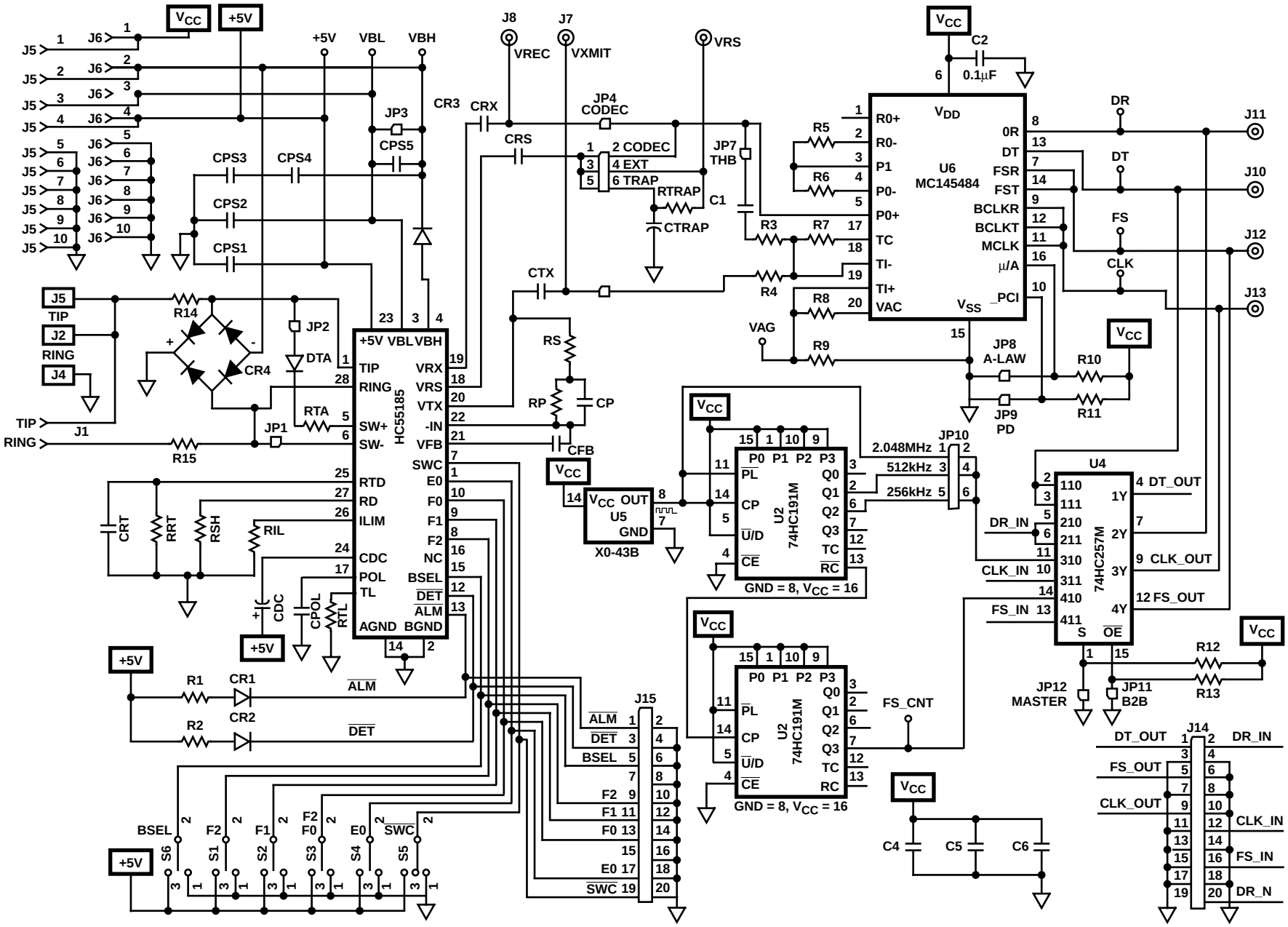
FIGURE 16. HC55185 BASIC APPLICATION CIRCUIT

Basic Application Circuit Component List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U1 - Ringing SLIC	HC55185	N/A	N/A	C_{DC}, C_{FB}	4.7µF	20%	10V
R_{RT}	20kΩ	1%	0.1W	C_{PS1}	0.1µF	20%	>100V
R_{SH}	49.9kΩ	1%	0.1W	C_{PS2}, C_{PS3}	0.1µF	20%	100V
R_{IL}	71.5kΩ	1%	0.1W	D_1	1N400X type with breakdown > 100V.		
R_S	66.5kΩ	1%	0.1W	R_{P1}, R_{P2} = 50Ω, 0.5W, matched to 0.1Ω.	Protection resistor values are application dependent and will be determined by protection requirements. Standard applications will use ≥ 50Ω per side.		
R_{TL}	17.8kΩ	1%	0.1W				
C_{RX}, C_{RS}, C_{TX}, C_{RT}, C_{POL}	0.47µF	20%	10V				

Design Parameters: Ring Trip Threshold = $90mA_{PEAK}$. Switch Hook Threshold = 12mA, Loop Current Limit = 24.6mA, Transient current limit: I_{SOURCE} = 100mA, I_{SINK} = 120mA, Synthesize Device Impedance = 66.5KΩ/133.3 = 500Ω, with 51Ω protection resistors, impedance across Tip and Ring terminals = 603Ω.

Evaluation Board Schematic



HC5518XEVAL Electrical Component List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U_1 - Ringing SLIC	HC5518x	N/A	N/A	R_3, R_7	100kΩ	1%	0.10W
U_2, U_3	74HC191M	N/A	N/A	R5, R6, R8, R9, R10, R11, R12, R13	10kΩ	1%	0.10W
U_4	74HC257M	N/A	N/A	R14, R15	51Ω	5%, picked to 0.1Ω	0.50W
U_5	XO-43B	N/A	N/A	CRT, CRX, CRS, CTX, C1, CPOL, CTRAP	0.47µF	20%	20V
U_6	MC145484DW	N/A	N/A	CDC, CFB	4.7µF	20%	20V
R_{RT}, R_{TRAP}	20kΩ	1%	0.10W	CPS1, CPS2, CPS3, CPS4, CPS5	0.1µF	20%	100V
R_{SH}	49.9kΩ	1%	0.10W	C2, C3, C4, C5, C6	0.1µF	20%	20V
R_{IL}	71.5kΩ	1%	0.10W	CR3	DL4003CT-ND	N/A	N/A
R_{TA}	100Ω	1%	0.25W	DTA	BAS21ZXCT	N/A	N/A
R_S	66.5kΩ	1%	0.10W	CR1, CR2	LN1251C	N/A	N/A
R_P	0Ω	1%	0.10W	R4	44.2kΩ	1%	0.10W
R_1, R_2	499Ω	1%	0.10W	RTL	17.8kΩ	1%	0.10W

HC5518XEVAL Mechanical Component List

COMPONENT	VALUE	TOLERANCE	RATING	COMPONENT	VALUE	TOLERANCE	RATING
U_1- Socket	822271-1	N/A	N/A	J14, J15	10 Pin Header	N/A	N/A
U_6 Socket	IC51-0202-347	N/A	N/A	J2, J3, J4	39F893	N/A	N/A
J5, J6	43045-1000	N/A	N/A	JP5, JP10	3 Pin Header	N/A	N/A
J1	555165-1	N/A	N/A	JP1, JP2, JP3, JP4, JP6, JP7, JP8, JP9, JP11, JP12	1 Pin Header		
J7, J8, J9, J10, J11, J12, J13	CBJR20	N/A	N/A	S1, S2, S3, S4, S5, S6	65F1681	N/A	N/A

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil Ltd.
8F-2, 96, Sec. 1, Chien-kuo North,
Taipei, Taiwan 104
Republic of China
TEL: 886-2-2515-8508
FAX: 886-2-2515-8369